AMENDMENTS TO CLAIMS

1. **(Currently Amended)** A buffer control apparatus in a buffered switch for controlling transmission of ~~packets/frames of~~ data, comprising:

a ~~dual port~~ buffer memory for storing the ~~packets/frames of~~ data;

a buffer write module for writing ~~packets/frames~~ the data into the ~~dual port~~ buffer memory;

a buffer read module for reading ~~packets/frames of~~ the data from the ~~dual port~~ buffer memory; ~~and~~

a deferred queue containing entries having destination and buffer address information for data to be deferred, with entries for data addressed to multiple destinations ports being intermingled within the deferred header queue;

a header select device for controlling the buffer read module and having an initial and a deferred state,

the initial state adding entries to the deferred queue so as to temporarily defer transmission ~~of the packets/frames~~ to a destination port ~~which is~~ unavailable to receive the ~~packets/frames~~ data, and

the deferred state processing all entries in the deferred header queue in the order in which the entries were written in the deferred header queue, the deferred state submitting the buffer address information for an entry to the buffer read module when the destination port is available to receive data or the deferred state keeping the buffer address information on the deferred header queue when the destination port is unavailable to receive data.

2-3. **(Cancelled)**

4. **(Currently Amended)** The buffer control apparatus according to claim 1 ~~3~~, wherein the ~~deferred queue~~ header select device ~~is in one of an Initial State, a Deferred State, and a Backup State~~ further has a backup state wherein data received during the deferred state is analyzed for transmission or deferral after the deferred state has reviewed all entries in the deferred header queue.

5. **(Currently Amended)** The buffer control apparatus according to claim 4 ~~3~~, ~~wherein the buffer control device~~ further ~~comprises~~ comprising:

a backup header queue ~~device for storing frame information for packets/frames waiting to be sent to at least one destination port because the packets/frames~~ containing entries for data that arrived ~~at an input port while deferred packets/frames were being sent to the at least one destination port~~ during the deferred state.

6. (**Cancelled**)

7. (**Currently Amended**) The buffer control apparatus according to claim 1 ~~3~~, wherein an XOFF ~~masks are~~ mask is used to determine the current status of all destination ports in the buffered switch, the XOFF mask being a memory device having a bit associated with each possible destination ports, with each bit indicating either the ability or inability of the destination port to receive data.

8. (**Currently Amended**) The buffer control apparatus according to claim 1 ~~3~~, wherein the ~~stored frame information~~ deferred queue entries each comprises ~~frame~~ header information for a data frame and a starting address in the buffer memory for the ~~packet/~~ data frame.

9. (**Currently Amended**) The buffer control apparatus according to claim 5, wherein the ~~stored frame information~~ backup header queue entries each comprises ~~frame~~ header information for a data frame and a starting address in the buffer memory for the ~~packet/~~ data frame.

10. (**Currently Amended**) A deferred queue device for temporarily deferring transmission of packets/frames to a destination port in a buffered switch, comprising:

a deferred header queue device for storing frame information for packets/frames being deferred, the deferred header queue device containing packets/frames addressed to more than one destination port;

means for periodically determining current status of all destination ports in the buffered switch; and

header select logic unit for determining state of the deferred queue device and supplying a valid buffer address for a deferred packet/frame which can now be sent to an available destination port.

11. (**Currently Amended**) The deferred queue device according to claim 10, wherein the deferred queue device further comprises a state engine can be in one of an Initial State, a Deferred State, and a Backup State.

12. (**Original**) The deferred queue device according to claim 10, further comprising: a backup header queue device for storing frame information for packets/frames waiting to be sent to at least one destination port because the packets/frames arrived at an input port while deferred packets/frames were being sent to the at least one destination port.

13. (**Currently Amended**) The deferred queue device according to claim 10, further comprising: a backup header queue device that operates in parallel with the deferred header queue for storing frame information for packets/frames waiting to be sent to at least one destination port.

14. (**Currently Amended**) The deferred queue device according to claim 10, wherein an XOFF ~~masks are~~ mask is used to determine the current status of all destination ports in the buffered switch, the XOFF mask being a memory device having a bit associated with each possible destination ports, with each bit indicating either the ability or inability of the destination port to receive data.

15. (**Cancelled**)

16. (**Original**) The buffer control apparatus according to claim 10, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame.

17. (**Original**) The buffer control apparatus according to claim 12, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame.

18. (**Currently Amended**) A method for temporarily deferring transmission of ~~packets/frames~~ data to a destination port in a buffered switch, comprising the steps of:

    a. during an initial state:

        i. receiving a request for transmission of ~~at least one packet/frame~~ data to the destination port;

        ii. determining whether the destination port is available to receive the ~~at least one packet/frame~~ data;

        iii. deferring transmission of the ~~at least one packet/frame~~ data when the determining step determines that the destination port is not available to receive the ~~at least one packet/frame~~ data by storing the data in a deferred queue whereby data addressed to different

destination ports are simultaneously stored in the same deferred queue;

iv. transmitting data to the destination port when the determining step determines the destination port is available to receive the data; and

v. repeating the above steps i-iv for ~~a next packet/frame~~ all data to be transmitted.

b. upon receiving notification that a destination port has changed state and may now receive data, entering into a deferred state during which:

i. all entries in the deferred queue are analyzed in the order in which the entries are added to the deferred queue;

ii. upon determining that the destination port for a data entry in the deferred queue is now able to receive data, transmitting the data to the destination port;

iii. upon determining the destination port for a data entry in the deferred queue is still not able to receive data, ensuring the data remains in the deferred queue; and

iv. repeating steps i-iii for all entries in the deferred queue.

19-22. (**Cancelled**)

23. (**Currently Amended**) The method according to claim 18 ~~19~~, further comprising the steps of: storing ~~packet/frame identifier and memory address~~ in a backup ~~header~~ queue ~~for packets/frames which are~~ entries for data received ~~while a~~ during the deferred state; ~~packet/frame is being sent to the destination port;~~ and further comprising the steps of:

c. upon completing step b, entering a backup state whenever there is data in the backup queue by performing the steps of:

i. periodically checking to determine if the destination ports for ~~packets/frames~~ data in the backup ~~header~~ queue are available;

ii. transmitting the ~~packets/frames~~ data to the destination ports when it is determined that the destination ports are available;

iii. ~~removing frame/packet identifier and memory address for transmitted packets/frames from the backup header queue~~ placing the data in the deferred queue when it is determined that the destination ports are not available.

24. (**Currently Amended**) The method according to claim 23, wherein ~~each frame/packet identifier~~ the data is transmitted to the destination port ~~based on first packet~~ in the order in which the data was received at the backup header ~~queue~~ for the destination port.

25. (**New**) The method of claim 18, wherein the deferred queue comprises a header queue containing header information for all data in the queue, the header information containing destination information and a buffer address location indicating where the data resides in a buffer memory.

26. (**New**) A data switch having a plurality of output ports, each output port having a positive or negative transmission status; the switch comprising:

a. an input buffer receiving a plurality of data frames each associated with anoutput port;

b. a mechanism at each input buffer to determine the transmission status of the output ports;

c. a deferred queue in which data for a plurality of different output ports having a negative transmission status is tracked;

d. a backup queue in which newly received data is queued when data in the deferred queue is being processed; and

e. a state machine that enters a deferred state when an output port moves from a negative to a positive transmission status, the deferred state causing the data switch:

i. to process data in the deferred queue so as to transmit to the associated output port that data which is addressed to an output port that now has a positive transmission status,

ii. to ensure that data in the deferred queue addressed to output ports that still have a negative transmission status remain in the deferred queue, and

iii. to place newly received data in the backup queue.

27. (**New**) The data switch of claim 26, wherein the state machine enters a backup state when all data in the deferred queue is processed in the deferred state and data exists in the backup queue, the backup state causing the data switch to determine whether the data in the backup queue should be transmitted to its

associated output ports or stored in the deferred queue based upon the transmission status of the data's associated output port.

28. (**New**) The data switch of claim 27, wherein the state machine moves from the backup state to the deferred state when an output port moves from the negative transmission state to the positive transmission status.

29. (**New**) The data switch of claim 28, wherein the state machine enters a normal state when the deferred state is completed and no data exists in the backup queue, or when the backup state is completed and no port has moved from the negative transmission state to the positive transmission state, and wherein the normal state causes the data switch to determine whether incoming data should be transmitted to the associated output port or queued on the deferred queue depending on the transmission status of the associated output port.

30. (**New**) The data switch of claim 26, wherein the mechanisms to determine the transmission status of the output ports is an XOFF mask.

31. (**New**) The data switch of claim 30, wherein the XOFF mask comprises a memory device having a bit associated with every output port, with each bit indicating either the ability or inability of the output port to receive data at a current time.

32. (**New**) The data switch of claim 30, wherein the XOFF mask is updated in real time except during the deferred state, during which time changes to the XOFF mask indicating a change of a port transmission status from negative to positive are delayed until all entries in the deferred queue have been analyzed.

33. (**New**) The data switch of claim 32, wherein the deferred state is reentered with an updated XOFF mask after all entries in the deferred queue are analyzed with an original XOFF mask if the change of a port transmission status from negative to positive occurs during the deferred state.

34. (**New**) The data switch of claim 26, wherein the data frames are selected from a group of frames comprising fixed length frames and packets, frames and packets having end of frame delimiters, and variable length data frames and packets.

35. (**New**) A data switch having a plurality of destination ports comprising:
a deferred queue that stores data being deferred, the deferred queue means containing data addressed to more than one destination port; and
a logic unit having an initial state and a deferred state,

in the initial state the logic unit transmits data to non-blocked destination ports and adds data to the deferred queue where that data is addressed to a blocked destination port, and

in the deferred state the logic unit processes data in the deferred queue by transmitting to its destination port that deferred data that is addressed to a no longer blocked destination port, and by retaining within the deferred queue data that is addressed to a still-blocked destination port.